CLAIMS

What is claimed is:

1. An apparatus comprising:

a sample/hold circuit having an input to receive an analog input voltage;

a comparator device coupled to said input of said sample/hold circuit to receive said analog input voltage; and

a separate gain circuit coupled to an output of said sample/hold circuit and to said comparator device;

said sample/hold circuit and said comparator device to sample said analog input voltage and said separate gain circuit to amplify an analog residue voltage obtained from said analog input voltage to obtain an amplified analog residue voltage in a first phase of a non-overlapping clock.

2. The apparatus according to claim 1, wherein said analog residue voltage is obtained in a second phase of said non-overlapping clock, when said sample/hold circuit holds said analog input voltage sampled in said first phase, and said comparator device compares said analog input voltage sampled in said first phase with a reference voltage value.

3. The apparatus according to claim 2, wherein said first phase and said second phase of said clock have unequal timing periods.

4. The apparatus according to claim 3, wherein said first phase timing period is longer than said second phase timing period.

5. The apparatus according to claim 1, wherein said separate gain circuit amplifies said analog residue voltage over said entire first phase of said clock.

6. An apparatus for performing analog-to-digital pipeline conversion, said apparatus comprising

a plurality of conversion stages , each conversion stage comprising:

a sample/hold circuit having an input to receive an analog input voltage from a prior adjacent conversion stage of said plurality of conversion stages;

a comparator device coupled to said input of said sample/hold circuit to receive said analog input voltage; and

a separate gain circuit coupled to an output of said sample/hold circuit and to said comparator device;

said sample/hold circuit and said comparator device to sample said analog input voltage and said separate gain circuit to amplify an analog residue voltage obtained from said analog input voltage to obtain an amplified analog residue voltage in a first phase of a non-overlapping clock, said gain circuit to

output said amplified analog residue voltage to a subsequent adjacent conversion stage of said plurality of conversion stages.

7. The apparatus according to claim 6, wherein said analog residue voltage is obtained in a second phase of said non-overlapping clock, when said sample/hold circuit holds said analog input voltage sampled in said first phase, and said comparator device compares said analog input voltage sampled in said first phase with a reference voltage value.

8. The apparatus according to claim 7, wherein said first phase and said second phase of said clock have unequal timing periods.

9. The apparatus according to claim 8, wherein said first phase timing period is longer than said second phase timing period.

10. The apparatus according to claim 6, wherein said separate gain circuit amplifies said analog residue voltage over said entire first phase of said clock.

11. A method comprising:

coupling a comparator device to an input of a sample/hold circuit in an analog-to-digital conversion apparatus; and

coupling a separate gain circuit to said comparator device and to an output of said sample/hold circuit;

said sample/hold circuit and said comparator device to receive an analog input voltage and to sample said analog input voltage,

and said separate gain circuit to amplify an analog residue voltage obtained from said analog input voltage to obtain an amplified analog residue voltage in a first phase of a non-overlapping clock.